Remarks

In the Office Action, Claims 1-3 and 5-9 were rejected as clearly anticipated under 35 U.S.C. §102(b) by Horden et al patent 5,812,860; and Claims 4 and 10-11 was rejected under 35 U.S.C. §103 as unpatentable over Horden. Claim 5 is being canceled by this amendment. Claims 1-4 and 6-11 remain in the application.

The Examiner rejected Claims 1-3 and 5-9 as clearly anticipated under 35 U.S.C. §102(b) by Horden. Claim 5 has been canceled, and Claims 1 and 6 have been amended to overcome the rejection. Withdrawal of the rejection as to the claims, as amended, is respectfully requested.

Applicant has invented an improved method and apparatus for reducing the power consumed by a computer processor. As applicants point out, it is desirable to use as little power as possible when operating a computer by reducing the frequency of operation of the processor and various other components associated with the processor to the minimum necessary to accomplish the operations being executed by the processor. As explained at page 2, line 22, through page 3, line 12, prior to the invention, this had been accomplished by one or more frequency generators, state machines or power management units, and power supplies al of which are external to and separate from the processor itself. Frequency generators which are external to the processor cause delays in crossing various interfaces, eliminated the ability to provide frequencies which may be changed in different ratios for different components, and generally slowed processing.

As will be seen by studying the Horden patent, this prior art apparatus and method is identical to what is disclosed in Horden (see Figure 1). Horden uses one or more external frequency generators 8, external power supplies 7 and voltage regulators 5, and external state machine 6.

The present invention improves on the prior art by providing a frequency generator on the same silicon chip as the processor. This eliminates the various interfaces which slow operation, allows direct control of the frequency by the processor itself, and facilitates the maintenance of a plurality of optimum frequencies for different components associated with the processor under control of the processor. None of these are possible utilizing prior art knowledge including that of Horden.

Horden does not suggest placing a frequency generator on a single chip with a processor. The only suggestion Horden makes is that the voltage regulator 5, clock generator 8, and state machine 6 may be placed on a single chip (see col. 3, lines 5-9). Although it might be assumed by a person not skilled in the art that it would be simple to provide a frequency generator on-chip with a processor to accomplish these things, that is not the case. It is very difficult to change frequency while the processor is executing instructions since changes in frequency require the frequency generator to lock and unlock without generating errors in operation (see discussion in applicants' specification beginning at page 9, line 5, and continuing on through first paragraph of page 16). An external frequency generator does not face this problem when there are two such generators. Nor does a single external frequency generator face this problem if the two conditions of operation are running and idle as Horden discusses (see col. 3, lines 37-47). Horden simply ignores the

problem. Horden does not consider how to accomplish frequency change with a single generator and two frequencies during which execution of instructions is accomplished.

A rejection for anticipation requires that all elements of the rejected claim be found in a single piece of prior art.

> "Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention, arranged as in the claim, Soundscriber Corp. v. U. S.,360 F.2d 954, 960 (Ct. Cl. 1966); Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379, 231 U.S.P.Q. 81,90 (Fed. Cir. 1986).

Horden does not show or teach an on-chip frequency generator.

Applicants' claims include (or have been amended to include) language requiring that the frequency generator be on-chip with the processor. For example, Claim 1, as amended recites:

> A method for controlling the operating condition of a computer processor on a chip including a clock generator comprising the steps of:

> determining a maximum allowable power consumption level from the operating condition of the processor,

> determining a maximum frequency which provides power not greater than the allowable power consumption level,

> determining a minimum voltage which allows operation at the maximum frequency determined, and

dynamically changing the operating condition of the processor by changing the frequency generated by the clock generator and the voltage to the maximum frequency and minimum voltage determined.

Since Horden does not disclose all of the claimed elements of the amended claims, Horden cannot anticipate the invention under 35 U.S.C. §102(b). The withdrawal of the rejection and the allowance of Claims 1-3 and 6-9, as amended, are, therefore, respectfully requested.

The Examiner rejected Claims 4 and 10-11 under 35 U.S.C. §103 as unpatentable over Horden. However, Horden cannot possibly be considered to teach, show, or otherwise suggest an on-chip frequency generator. This is clear because Horden suggests no method for changing between frequencies at both of which a processor is actually executing instructions. As may be seen at page 9, line 5, and continuing on through first paragraph of page 16 of applicants' specification, such a process is very complex and cannot in any manner be considered an obvious process.
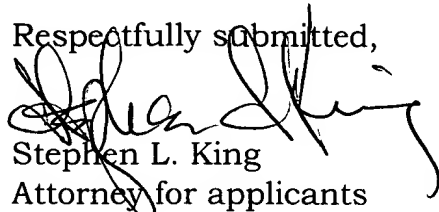
As the Federal Circuit has often held:

> "To invalidate a patent, there must have been something present in the teachings of a reference to suggest to one skilled in the art that the claimed invention would have been obvious, W. L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983)."

Since Horden does not teach, disclose, or suggest in any manner the on-chip frequency generator or how it might be utilized, the withdrawal of

the rejection of Claims 4 and 10-11, as amended, as obvious under 35 U.S.C. §103 is respectfully requested.

Since all claims now in the application appear to be allowable over the rejections included in the Office Action, the allowance of those claims, as amended, and the issuance of the application as a patent are respectfully requested.

Respectfully submitted,

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Stephen L. King
Attorney for applicants

30 Sweetbay Road
Rancho Palos Verdes, CA 90275
(310) 377-5073

Version with markings to show changes made:

Please amend the claims as follows:

1 Claim 1 (amended).   A method for controlling the operating condition

2 of a computer processor <u>on a chip including a clock generator</u> comprising

3 the steps of:

4 determining a maximum allowable power consumption level from the

5 operating condition of the processor,

6 determining a maximum frequency which provides power not greater

7 than the allowable power consumption level,

8 determining a minimum voltage which allows operation at the maximum

9 frequency determined, and

10 dynamically changing the operating condition of the processor by

11 changing the frequency <u>generated by the clock generator</u> and <u>the</u> voltage

12 to the maximum frequency and minimum voltage determined.

1 Cancel Claim 5.

1 Claim 6 (amended).   A method <u>for controlling the power used by a</u>

2 <u>computer comprising the steps of:</u>

3 <u>utilizing control software to measure the operating characteristics of a</u>

4 <u>central processor of the computer,</u>

5 <u>determining when the operating characteristics of the central processor</u>

6 <u>are significantly different than required by the operations being</u>

7 <u>conducted, and</u>

8 <u>changing the operating characteristics of the central processor to a level</u>

9 <u>commensurate with the operations being conducted</u> [as claimed in Claim

10 5] in which:

11 the step of determining when the operating characteristics of the central

12 processor are significantly different than required by the operations being

13 conducted comprising utilizing the control software to determine

•14 desirable voltages and frequencies for the operation of the central

15 processor based on the measured operating characteristics, and

16 the step of changing the operating characteristics of the central

17 processor to a level commensurate with the operations being conducted

18 comprises providing signals:

19 for controlling voltages furnished by a programmable power supply

20 to the central processor, and

21 for controlling frequencies furnished by the central processor to the

22 central processor.